

## METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

### FIELD OF THE INVENTION

The present invention relates to the field of semiconductors and, more particularly, to an improved dielectric for increasing semiconductor performance.

### CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a divisional of U.S. Patent Application Serial No. 10/273,667 filed October 18, 2002 which is a divisional of U.S. Patent Application Serial No. 09/653,096, filed August 31, 2000.

This application is related to commonly assigned U.S. Patent Application Serial Nos.: 09/653,639, METHOD FOR FORMING A BARRIER LAYER TO INCREASE SEMICONDUCTOR DEVICE PERFORMANCE, filed August 31, 2000, by Powell et al. and 09/653,298, METHOD FOR FORMING A DIELECTRIC LAYER AT A LOW TEMPERATURE, filed August 31, 2000, by Mercaldi et al., the disclosures of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

There is a constant demand for semiconductor devices of a reduced size. The performance characteristics of semiconductor capacitors, transistors, electrode layers and the like become more critical as device size decreases. Accordingly, processes that result in increased device performance are critical to improved semiconductor device fabrication.

Capacitors generally have two conductive layers or plates separated by an insulator layer or dielectric layer. Capacitor performance can be improved by increasing the dielectric constant of the dielectric material or decreasing the leakage characteristics of the dielectric material.

Accordingly, there is a need in the art for an improved dielectric layer that has improved characteristics such as lower leakage and a higher dielectric constant.

## SUMMARY OF THE INVENTION

This need is met by the present invention, where a silicon-containing material is deposited over at least a portion of a semiconductor device. The deposited silicon-containing material is processed in a reactive ambient to form the dielectric layer.

In accordance with one embodiment of the present invention, a method for fabricating a semiconductor device is disclosed.

According to the method, a substrate having at least one semiconductor layer is provided. A first conductive layer is formed over the substrate. A silicon-containing material is deposited over at least a portion of the semiconductor device. The deposited silicon-containing material is processed in a reactive ambient to form a dielectric layer. A second conductive layer is formed over the dielectric layer.

In accordance with yet another embodiment of the present invention, a semiconductor device is disclosed. The semiconductor device includes a substrate, a first conductive layer, a silicon-containing dielectric layer and a second conductive layer. The first conductive layer is formed over the substrate. The silicon-containing layer is formed over the first conductive layer by reacting silicon atoms from a precursor layer with a reactive agent. The second conductive layer is formed over the silicon-containing layer.

Other methods and devices are disclosed.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The following detailed description of the present invention can be best understood when read in conjunction with the accompanying drawings, where like structure is indicated with like reference numerals.

Figure 1 illustrates a method for forming a dielectric layer according to one embodiment of the present invention.

Figure 2 illustrates a method for forming a dielectric layer according to another embodiment of the present invention.

Figure 3B is a graphical illustration of capacitance versus leakage for various dielectric layers.

Figure 3C is a graphical illustration of capacitance versus breakdown voltage for various dielectric layers.

Figure 3D is a graphical illustration of the cumulative probability of leakage for various dielectric layers.

Figure 3E is a graphical illustration of the cumulative probability versus capacitance for various dielectric layers.

Figure 3F is a graphical illustration of the cumulative probability versus breakdown voltage.

Figure 3G is a graphical illustration of the performance index versus low level voltages for various dielectric layers.

Figure 3H is a graphical illustration of the performance index for various dielectric layers.

Figure 4 illustrates a semiconductor device according to another embodiment of the present invention.

Figure 5 illustrates use of a silicon-containing dielectric layer in a capacitor according to another embodiment of the present invention.

Figure 6 illustrates a computer system that can use and be used with embodiments of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates a method for forming a dielectric layer according to one embodiment of the present invention. A silicon-containing layer or precursor layer is deposited over a substrate at block 101. The silicon-containing layer includes material from a silazane or silane source such as, but not limited to hexamethyldisilazane (HMDS). A dielectric layer is formed by processing the silicon-containing layer in a reactive ambient 102. The reactive ambient can be comprised of, but not limited to,  $\text{NH}_3$ ,  $\text{N}_2$ ,  $\text{O}_2$ ,  $\text{O}_3$ ,  $\text{N}_2\text{O}$  and  $\text{NO}$ . The reactive ambient causes silicon atoms from the silicon-containing layer to react with oxygen atom, nitrogen atoms or both. The dielectric layer is primarily nitride, primarily oxide or oxynitride depending on whether the reactive ambient is nitridizing, oxidizing or nitridizing and oxidizing.

Generally, conventional dielectric layers are processed using temperature ranges of 700°C to 1050°C, processing time of 10 seconds to 60 minutes, and processing pressure of 760 torr. Whereas, the dielectric layer of the present invention is typically processed using temperature ranges of 500°C to 900°C, processing time of 30 seconds to 5 minutes, and processing pressure of 450 torr. However, with silicon sources such as HMDS, the time is not critical because they are self limiting sources. It is contemplated that variations to these ranges may also result in suitable dielectric layer formation.

Figure 2 illustrates a method of fabricating a silicon-nitride dielectric layer. A wafer is cleaned using hydrofluoric acid (HF) or any other suitable cleaning technique 201. A silicon-containing material, is vapor deposited over the wafer 202 from a silicon source such as HMDS. The silicon-containing material can be deposited using a vapor priming (VP) step. Conventionally, vapor priming is one method that has been used, for example, to minimize the amount of photoresist needed during a patterning process. The vapor prime helps "pre-wet" the semiconductor wafer and allows photoresist to flow out more smoothly, and thus more homogeneously. A dielectric layer is fabricated by rapid thermal nitridization (RTN) of the deposited

material in an ammonia nitrogen (NH<sub>3</sub>) ambient 203. The resulting dielectric layer is primarily nitride.

Split	Wafers	VP	RTN	Dielectric	Thickness
301	2	-	850°C	Nitride	45Å
302	4,16	-	-	Nitride	45Å
303	6,18	-	-	Nitride	55Å
306	14	1	850°C	Nitride	35Å
307	1,15	2	850°C	Nitride	35Å
308	3,17	2	850°C	Nitride	45Å
309	5,19	2	950°C	Nitride	35Å

TABLE 3A

Table 3A, shown above, shows experimental results for dielectric layers fabricated utilizing the method of figure 2A versus conventional dielectric layers. Here, each split represents a set of dielectric layers fabricated according to the same or similar parameters. Splits 302 and 303 are dielectric layers fabricated according to conventional means with a thickness of 45Å and 55Å, respectively. Splits 301 and 306-309 are dielectric layers formed according to the present invention.

Split 301 is a dielectric layer fabricated using RTN. Split 306 utilizes a single vapor priming (VP) step and a processing temperature of 850°C to fabricate a dielectric layer at a thickness of 35Å. Vapor priming or VP is used to deposit a layer of silicon-containing material. Splits 307-309 perform vapor priming twice to deposit two layers of silicon-containing material. Splits 307 and 308 are processed at a temperature of 850°C to form dielectric layers of 35Å and 45Å, respectively. Split 309 is processed at a temperature of 950°C to form a dielectric layer having a thickness of 35Å.

Figure 3B shows capacitance versus leakage for the dielectric layers of table 3A. The leakage is shown on a logarithmic scale. Split 302 demonstrates larger leakage than the other splits. The other splits are well grouped and have less than 7fA/Cell leakage. Thus, the present invention decreases leakage compared to conventional dielectric layers of comparable thickness.

Figure 3C shows capacitance versus BV (breakdown voltage to induce 1uA) for the dielectric layers of table 3A. This figure shows the BV of the 302 split at around 3.0V. This behavior in leakage and BV is indicative of 45Å nitride. The remaining splits demonstrate higher BV. It is worth noting that the less

thick splits, 306, 307 and 309 even demonstrate a higher BV. A higher BV indicates a large increase in dielectric strength. Thus, it can be seen that the present invention increases dielectric strength.

Figure 3D shows the cumulative probability of leakage for the dielectric layers of table 3A. The leakage probability of split 302 is unacceptable and all other splits are comparable to split 303, the 55Å thick control dielectric layer which is thicker than the other splits. Thus, it can be seen that the present invention lowers leakage probability of dielectric layers of comparable thickness. Figure 3E shows the cumulative probability versus capacitance. A 2.5fF/cell gap is seen between split 303 and the best remaining splits. Thus, it can be seen that the present invention demonstrates an increase in capacitance over conventional dielectrics. Similarly, figure 3F shows the cumulative probability versus BV and a significant gap between split 302 and the other splits. This shows that the dielectric layers of the present invention demonstrate improved back voltage characteristics over conventional dielectrics of comparable thickness.

Figure 3G shows a performance index C/I (capacitance over current) versus low level voltages for the dielectric layers of table 3A. The data for the graph was gathered using Keithley CV

and IV sweeps. The bias voltage was swept from +1V to -1V while measuring capacitance. The IV sweep swept bias voltage from 0 to -1V and measured 20K array current. The performance of the 302 split significantly degrades over a range of approximately 0.6V. This performance degradation is a result of leakage increases. The best performance of the splits is shown by split 307 which uses 2VP, a processing temperature of 850°C and a 35Å thickness. Figure 3H shows the performance index C/I for the various dielectric layers of table 3A. The vertical axis is the performance index C/I and the horizontal axis shows the various splits. The circles on the right hand side of the graph show the differences between the various dielectric layers. If the circles do not intersect, the difference between splits is significant. Splits 307, 308 and 309 are significantly better in performance than control splits 302 and 303.

Table 3A and figures 3B, 3C, 3D, 3E, 3F, 3G and 3H show exemplary experimental results of actual implementations. It can be seen from those figures that thinner dielectric layers fabricated according to the present invention are able to perform as well or better than thicker conventional dielectric layers. Other actual implementations may vary and embodiments of the

present invention are not limited to the implementations shown in table 3A and figures 3B, 3C, 3D, 3E, 3F, 3G and 3H.

Figure 4 illustrates a transistor semiconductor device utilizing a dielectric layer 402 according to another embodiment of the present invention. A source 405 is formed in a substrate 401. A drain 406 is formed in the substrate 401. A gate oxide layer 404 is formed over the substrate 401 from the source 405 to the drain 406. An electrode or gate electrode 403 is formed over the gate oxide layer 404. A dielectric layer 402 is formed over the electrode 403.

The dielectric layer 402 is fabricated by vapor depositing a selected material or precursor and subsequently processing those materials. The selected material can be deposited by using vapor priming (VP). The selected material is a silicon containing material such as silazane or silane type materials. An example of a typical silicon-containing material is hexamethyldisilazane (HMDS). Other materials or precursors which may be used are tetramethyldisilazane, octamethylcyclotetrasilazine, hexamethylcyclotrisilazine, diethylaminotrimethylsilane or dimethylaminotrimethylsilane. The selected material can be deposited a single time or the depositing can be repeated any number of times. The selected material is processed in a reactive ambient to create a final desirable silicon-containing

dielectric layer. The reactive ambient can be materials such as  $\text{NH}_3$ ,  $\text{N}_2$ ,  $\text{O}_2$ ,  $\text{O}_3$ ,  $\text{N}_2$ ,  $\text{NO}$  and the like and cause silicon atoms of the selected material to react with oxygen atoms, nitrogen atoms or both. The resulting silicon-containing dielectric layer is the dielectric layer 402 and can result in a layer that is primarily nitride, primarily oxide or an oxynitride.

Figure 5 illustrates use of a silicon-containing dielectric layer 502 in a capacitor according to another embodiment of the present invention. The silicon-containing dielectric layer 502 is formed over an electrode 501. The silicon-containing dielectric layer 502 is created by depositing a silicon-containing precursor material from a silazane or silane source. The layer is then processed in a reactive ambient. The reactive ambient causes silicon atoms in the precursor layer to react with oxygen atoms, nitrogen atoms or both to form the silicon-containing dielectric layer. A second dielectric layer 503 is formed over the silicon-containing dielectric layer 502. The second dielectric layer 503 may be of a material susceptible to oxygen migration such as  $\text{Ta}_2\text{O}_5$  and may be formed using conventional methods. The electrode 501 may be composed of a material such as P-Si, SiGe or metal. The remaining capacitor structure is formed according to conventional methodology.

Figure 6 is an illustration of a computer system 612 that can use and be used with embodiments of the present invention. As will be appreciated by those skilled in the art, the computer system 612 would include ROM 614, mass memory 616, peripheral devices 618, and I/O devices 620 in communication with a microprocessor 622 via a data bus 624 or another suitable data communication path. The ROM 614 and mass memory 616 can be fabricated using silicon-containing dielectric layers according to the various embodiments of the present invention.

For the purposes of describing and defining the present invention, formation of a material "on" a substrate or layer refers to formation in contact with a surface of the substrate or layer. Formation "over" a substrate or layer refers to formation above or in contact with a surface of the substrate. A "substrate" may comprise one or more semiconductor layers or semiconductor structures which may define portions of a semiconductor device.

Dielectric layers fabricated using the present invention can be used for a variety of purposes. Some examples follow, but embodiments of the present invention are not limited to these. A dielectric layer can be used as a covering on a semiconductor device. A dielectric layer according to the present invention can be used in a gate structure of a transistor or in an anti-

fuse application. A dielectric layer according to the present invention can be formed on top of metals to prevent oxidation of metals. A dielectric layer according to the present invention can be used in post gate stack and pre oxidation steps to prevent oxygen in-diffusion into active areas of the transistor. A dielectric layer according to the present invention can be used to prevent oxidation of gate electrodes with subsequent processing steps when using materials such as polysilicon, Si-Ge, W or other transistor metals. A dielectric layer according to the present invention can be used in anti-fuse components of a semiconductor device.

Additionally, multiple dielectric layers formed according to the various embodiments of the present invention can be used in a single device and can be stacked or intermixed with other types of dielectric layers.

Semiconductor devices fabricated utilizing the present invention can be improved compared to other semiconductor devices because the dielectric of this invention can provide an increased dielectric constant and reduced leakage. This may also permit reductions in the size of semiconductor devices.

Having described the present invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing

Attorney Docket No.:  
MIO 0060 V3/ 98-0814.03

from the scope of the present invention defined in the appended  
claims.